ABSTRACT

A design method for automatically determining layout of a multilayer semiconductor device which has circuit blocks formed on a semiconductor substrate and measurement terminals for measuring voltage, logic state, or the like, on wiring lines for connecting the circuit blocks. The method includes the steps of registering measurement terminals as cells in design rules, together with the circuit blocks. wherein each measurement terminal has an electrode formed in an uppermost layer of the semiconductor device, and the measurement terminal is connectable to a wiring line for connecting any two of the circuit blocks, which is formed in any layer of the semiconductor device; planar-arranging the measurement terminals and the circuit blocks; and establishing connection of each wiring line, which extends from one of the circuit blocks, via one of the measurement terminals.